Amendments to the Specification:

Please replace paragraph 21 with the following amended paragraph:

[21] The flexibility afforded by the I/O architecture of the present invention speeds up the time-to-market cycle for new and larger PLDs. When designing a next generation PLD, because of the uncertainty regarding the eventual die size as well as the package hardware restrictions, the designer is unable to decide on the location of DQ and DQS pins until the end of the design cycle. This adds further delays to the design cycle. The present invention essentially eliminates this delay by providing a modular I/O architecture that [is] can be easily scaled such that the boundaries of each I/O section can still be defined at an early design stage. According to one embodiment of the invention, the DDR I/O section may have a number of I/O registers that is larger than the minimum (e.g., 8) required for a particular multiple-data-rate (e.g., DDR) system. With pre-defined boundaries, however, the sections can be placed while final DQS locations can be decided at a later time from one of multiple possible pins in the DDR I/O section followed by the DQ and local clock net. ~~[Philip, assuming this requires ALL I/O cells to be identical in resources, does that mean that each one is equipped with the phase delay circuit also? If not, how can the designer select the DQS pin to be any among the whole section?]~~